

OCT 21 2004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application Serial No. 10/749,659
Filing Date December 30, 2003
Inventor Zhongze Wang
Assignee Micron Technology, Inc.
Group Art Unit 2812
Examiner Jennifer M. Kennedy
Attorney Docket No. MI22-2477
Customer No. 021567
Title Silicon-on-Insulator Comprising Integrated Circuitry

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

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3. Statement of the Substance of the Interview

Dated: 10/21/04By: Pat Palmer

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Application Number

10749,659

Filing Date

December 30, 2003

First Named Inventor

Zhongze Wang

Art Unit

2812

Examiner Name

Jennifer M. Kennedy

Attorney Docket Number

M122-2477

ENCLOSURES (Check all that apply)

Fee Transmittal Form



Fee Attached



Amendment/Reply



After Final



Affidavits/declaration(s)



Extension of Time Request



Express Abandonment Request



Information Disclosure Statement



Certified Copy of Priority Document(s)

Reply to Missing Parts/
Incomplete ApplicationReply to Missing Parts
under 37 CFR 1.52 or 1.53

Drawing(s)



Licensing-related Papers



Petition

Petition to Convert to a
Provisional ApplicationPower of Attorney, Revocation
Change of Correspondence Address

Terminal Disclaimer



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After Allowance Communication to TC

Appeal Communication to Board
of Appeals and InterferencesAppeal Communication to TC
(Appeal Notice, Brief, Reply Brief)

Proprietary Information



Status Letter

Other Enclosure(s) (please identify
below):Certificate of Facsimile Transmission;
Statement of the Substance of the Interview
(of 10/18/04)

Remarks

Customer No. 021567.

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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name

Wells St. John P.S.

Signature

Printed name

Mark S. Matkin

Date

10/21/04

Reg. No.

32,268

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STATEMENT OF THE SUBSTANCE OF THE INTERVIEW

To: Commissioner for Patents
ATTENTION: Examiner Jennifer M. Kennedy
Group Art Unit 2812
P. O. Box 1450
Alexandria, VA 22313-1450

VIA FACSIMILE

From: Mark Matkin (Tel. 509-624-4276; Fax 509-838-3424)
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An interview was conducted between the undersigned and Examiner Kennedy on October 18, 2004.

It was agreed during the interview that claims 11 and 62 as presented below would be allowable (subject to further searching), and that such amendments would be made/entered by the Examiner by an "Examiner's Amendment".

11. Silicon-on-insulator comprising integrated circuitry, comprising:

a substrate comprising a semiconductive silicon comprising layer of silicon-on-insulator circuitry, the silicon comprising layer comprising a pair of source/drain regions formed therein and a channel region formed therein which is received intermediate the source/drain regions;

a transistor gate received operably proximate the channel region; and

an insulator layer of the silicon-on-insulator circuitry received on the silicon comprising layer, the insulator layer comprising a first silicon dioxide comprising region in contact with the silicon comprising layer and running along ~~only a portion~~ at least a portion of the channel region between the source/drain regions, a silicon nitride comprising region in contact with the first silicon dioxide comprising region and running along ~~at least a portion~~ only a portion of the channel region, and a second silicon dioxide comprising region in contact with the silicon nitride comprising region, the silicon nitride comprising region being received intermediate the first and second silicon dioxide comprising regions.

62. Silicon-on-Insulator comprising integrated circuitry, comprising:

a substrate comprising a semiconductive silicon comprising layer of silicon-on-insulator circuitry, the silicon comprising layer comprising a pair of source/drain regions formed therein and a channel region formed therein which is received intermediate the source/drain regions;

a transistor gate received operably proximate the channel region; and

an insulator layer of the silicon-on-insulator circuitry received on the silicon comprising layer, the insulator layer comprising a first silicon dioxide comprising region in contact with the silicon comprising layer and running along ~~only a portion~~ at least a portion of the channel region between the source/drain regions, a silicon oxynitride comprising region in contact with the first silicon dioxide comprising region and running along ~~at least a portion~~ only a portion of the channel region, and a second silicon dioxide comprising region in contact with the silicon oxynitride comprising region, the silicon oxynitride comprising region being received intermediate the first and second silicon dioxide comprising regions.

Respectfully submitted,

Dated: 10-21-04


Mark S. Matkin, Reg. No. 38,268